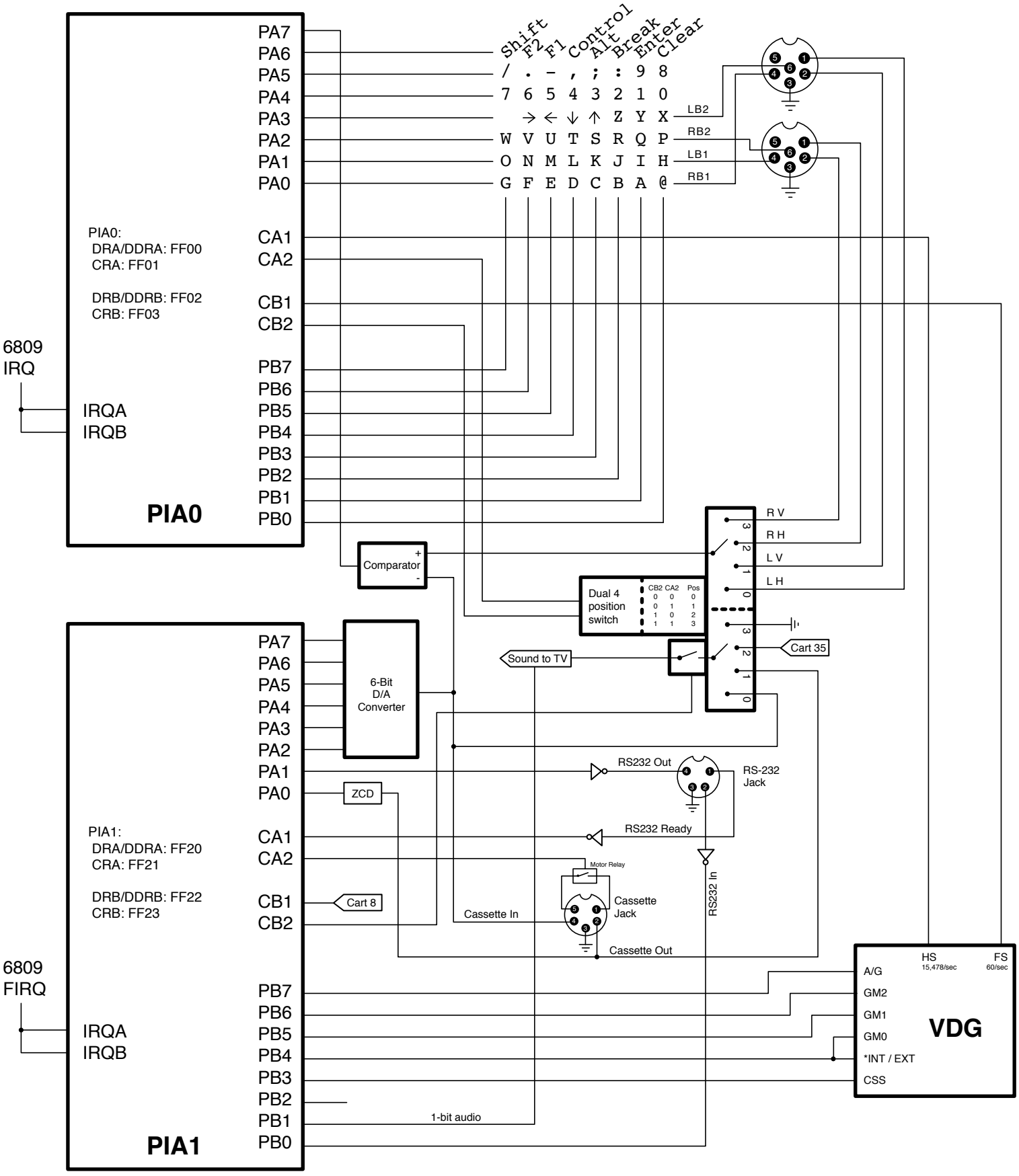
Color Computer PIAs



MC6821 Control Register A (B)

Determine Active CA1 (CB1) Transition for Setting Interrupt Flag IRQA(B)1 — (bit 7)

b1=0: IRQA(B)1 set by high-to-low transition on CA1 (CB1).

b1=1: IRQA(B)1 set by low-to-high transition on CA1 (CB1).

IRQA(B) 1 Interrupt Flag (bit 7)

Goes high on active transition of CA1 (CB1). Automatically cleared by MPU Read of Output Register A (B). May also be cleared by hardware Reset.

CA1 (CB1) Interrupt Request Enable/Disable

b0=0: Disables IRQA(B) MPU Interrupt by CA1 (CB1) active transistion.[1]

b0=1: Enables IRQA(B) MPU Interrupt by CA1 (CB1) active transistion.

1. IRQA(B) will occur on next (MPU generated) positive transition of b0 if CA1 (CB1) active transition occured while interrupt was disabled.

	b7	b6	b5	b4	b3	b2	b1	b0
Control Register	IRQA(B)1 Flag	IRQA(B)2 Flag	CA2 (CB2) Control			DDRA (B) Access	CA1 (CB1) Control	

IRQA(B) 2 Interrupt Flag (bit 6)

When CA2 (CB2) is an input, IRQA(B) goes high on active transition CA2 (CB2): Automatically cleared by MPU Read of Output Register A(B) May also be cleared by hardware Reset.

CA2 (CB2) Established as Output (b5=1): IRQA(B)2=0, not affected by CA2 (CB2) transitions.

Determines Whether Data Direction Register Or Output Register is Addressed

b2=0: Data Direction Register selected.

b2=1: Output Register selected.

CA2 (CB2) Established as Output by b5 = 1

(Note that operation of CA2 and CB2 output functions are not identical)

b5 b4 b3

1 0 → CA2

b3=0: **Read Strobe with CA1 Restore**
CA2 goes low on first high-to-low E transition following an MPU read of Output Register A; returned high by next active CA1 transition, as specified by bit 1.

b3=1: **Read Strobe with E Restore**
CA2 goes low on first high-to-low E transition following an MPU read of Output Register A; returned high by next high-to-low E transition during a deselect.

→ CB2

b3=0 **Write Strobe with CB1 Restore**
CB2 goes low on first low-to-high E transition following an MPU write into Output Register B; returned high y the next active CB1 transition as specified by bit 1. CRB-b7 must first be cleared by a read of data.

b3=1 **Write Strobe with E Restore**
CB2 goes low on first low-to-high E transition following an MPU write into Output Register B; returned high by the next low-to-high E transition following an E pluse which occured while the part was deselected.

b5 b4 b3

1 1 → **Set/Reset CA2 (CB2)**
CA2 (CB2) goes low as MPU writes b3=0 into Control Register
CA2 (CB2) goes high as MPU writes b3=1 into Control Register

CA2 (CB2) Established as input by b5 = 0

b5 b4 b3

0 → **CA2 (CB2) Interrupt Request Enable/Disable**

b3=0: Disables IRQA(B) MPU interrupt on CA(2) (CB2) active transisition.*

b3=1: Enables IRQA(B) MPU interrupt on CA(2) (CB2) active transisition.

→ **Determines Active CA2 (CB2) Transition for Setting Interrupt Flag IRQA(B)2 – (Bit b6)**

b4=0 IRQA(B)2 set by high-to-low transition on CA2 (CB2).

b4=1 IRQA(B)2 set by low-to-high transition on CA2 (CB2).

DDRA (DDRB)

bx

→ **Data Direction Register**

bx=0: Input

bx=1: Output